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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Hiroyuki Nitta et al.	) Group Art Unit: 2815
Serial No. 09/883,210	) Examiner: J. Nguyen
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For: SEMICONDUCTOR DEVICE HAVING A WIRING LAYER OF DAMASCENE STRUCTURE AND METHOD FOR MANUFACTURING THE SAME	) Atty. Dkt. No. 001701.00086

SUBMISSION OF TRANSLATION

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Arlington, VA 22202

Sir:

Applicants submit herewith the English translation of Japanese Application No. 2000-185152 filed on June 20, 2000.

No fees are believed to be associated with the filing of this submission. However, if the Commissioner should determine otherwise, please charge our Deposit Account No. 19-0733 the appropriate fee(s).

Respectfully Submitted,

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FOR: SEMICONDUCTOR DEVICE HAVING A WIRING LAYER OF DRAMASCENE STRUCTURE AND METHOD FOR MANUFACTURING THE SAME

TRANSLATION OF DOCUMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Kenji Kobayashi, a translator residing at 2-46-10, Gokonishi, Matsudo-shi, Chiba-ken, Japan, hereby states:

(1) that I know well both the Japanese and English languages;

(2) that I translated the attached document identified as corresponding to Patent Application No. 2000-185152 filed in Japan on June 20, 2000 from Japanese to English;

(3) that the attached English translation is a true and accurate translation to the best of my knowledge and belief.

DATE: December 13, 2004

BY: Kenji Kobayashi
Kenji Kobayashi

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[Title of the Invention] SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

[Number of Claims] 10

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[Name of Item]	Specification	1
[Name of Item]	Drawing	1
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[Title of the Invention] SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

[What is claimed is:]

[Claim 1] A semiconductor device characterized by comprising:

an insulation film provided above a semiconductor substrate;

a conductive film selectively provided at least on a bottom of a groove section formed in the insulation film; and

a wiring layer formed on the conductive film so as to have a space region between the wiring layer and a sidewall of the groove section.

[Claim 2] The semiconductor device according to claim 1, characterized in that the conductive film has resistivity that is higher than that of the wiring layer.

[Claim 3] A semiconductor device characterized by comprising:

an insulation film provided above a semiconductor substrate;

a wiring layer buried in the insulation film;

a first conductive film provided on a bottom of the wiring layer; and

a second conductive film formed on a sidewall of the wiring layer, and different from the first conductive film.

[Claim 4] The semiconductor device according to claim 3, characterized in that the second conductive film is made from a material different from that of the wiring layer.

[Claim 5] A semiconductor device characterized by

comprising:

a first insulation film provided above a semiconductor substrate;

a wiring layer buried in the first insulation film;

a first conductive film provided on a bottom of the wiring layer; and

a second insulation film formed on a sidewall of the wiring layer and different from the first insulation film.

[Claim 6] A semiconductor device characterized by comprising:

a first insulation film provided above a semiconductor substrate;

a wiring layer buried in the first insulation film;

a first conductive film provided on a bottom of the wiring layer; and

a contact plug formed via the wiring layer and the second insulation film that is different from the first insulation film.

[Claim 7] A method of manufacturing a semiconductor device, characterized by comprising the steps of:

forming an insulation film above a semiconductor substrate;

forming a groove section in the insulation film;

forming a conductive film along the interior surface of the groove section;

forming a wiring layer by burying a first conductive material in the groove section via the conductive film; and

selectively removing the conductive film formed on

sidewall portions of the groove section.

[Claim 8] The method of manufacturing a semiconductor device according to claim 7, characterized by further comprising the steps of: forming a second insulation film on the insulation film; and forming a space region between the wiring layer and the sidewall of the groove section from which the conductive film is removed.

[Claim 9] The method of manufacturing a semiconductor device according to claim 7, characterized by further comprising the step of burying a second conductive material in a region between the wiring layer and a sidewall of the groove section from which the conductive film is removed.

[Claim 10] A method of manufacturing a semiconductor device, characterized by comprising the steps of:

forming a first insulation film above a semiconductor substrate;

forming a groove section in the first insulation film;

forming a second insulation film on the interior surface of the groove section;

forming a conductive film along the interior surface of the groove section;

forming a wiring layer by burying a conductive material in the groove section via the conductive film; and

removing the second insulation film.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor device

and a method for manufacturing the semiconductor device, and particularly to wiring having a damascene structure.

[0002]

[Prior Art]

Miniaturization of semiconductor devices has recently been advanced to make a wiring layer difficult to form by conventional RIE (Reactive Ion Etching). This difficulty is ascribed to difficulties in improvement of yields and flattening when a conductive film is fabricated by the RIE.

[0003]

As a technique of resolving this problem, a wiring of damascene structure (hereinafter referred to as a damascene wiring) has been known conventionally.

[0004]

FIG. 9 schematically shows a process of manufacturing a prior art damascene wiring. First, for example, an interlayer insulation film 101 is formed on a semiconductor substrate (not shown) and a wiring pattern groove 103 is formed in the interlayer insulation film 101 by known lithography and RIE (see FIG. 9(a)).

[0005]

Then, a barrier metal film 105 is deposited on the entire surface. A conductive film 107 is deposited on the barrier metal layer 105 to completely fill the groove 103 (see FIG. 9(b)).

[0006]

After that, using CMP (Chemical Mechanical Polishing), the conductive film 107 and the barrier metal film 105 are

removed except for the interior portion of the groove 103 to form a flat surface, thereby obtaining a damascene wiring 109 (see FIG. 9(c)).

[0007]

A multilevel wiring can be formed if the above-described process is repeated.

[0008]

However, with the conventional method described above, it is necessary to deposit titanium nitride (TiN), niobium (Nb) and the like as a barrier metal when burying tungsten (W), aluminum (Al) and the like as a conductive film. This barrier metal increases in adhesion to the interlayer insulation film of W and serves as a glue layer or a barrier layer in reflowing of Al.

[0009]

The resistivity of the barrier metal is generally higher than that of the conductive film. Therefore, the prior art semiconductor device described above had a problem that the resistance of the damascene wiring was higher than a wiring formed by the RIE method (referred to as an RIE wiring hereinafter).

[0010]

FIG. 10 illustrates a damascene wiring and an RIE wiring formed having the same line width L for purposes of comparison.

[0011]

In the damascene wiring 109 shown in FIG. 10(a), the barrier metal film 105 is formed on each sidewall of the conductive film 107. Thus, the width L' of the conductive film

107 is smaller than the line width L of the damascene wiring 109 by two times (2b) the thickness of the barrier metal film 105 (L' = L - 2b < L).

[0012]

In the RIE wiring 201 shown in FIG. 10(b), the film width L' of the conductive film 107 is equal to the line width L of the RIE wiring 201 (L' = L).

[0013]

In other words, the cross-sectional area (volume) of the conductive film 107 in the damascene wiring 109 is relatively smaller than that in the RIE wiring 201.

[0014]

The thickness (b) of the barrier metal film 105 is determined appropriately to serve as a glue layer for forming the conductive film 107, to secure adhesion enough, or to obtain good characteristics of contact with the other layer. In short, the barrier metal film 105 having a given thickness or more is indispensable for forming the damascene wiring 109.

[0015]

If the damascene technique is applied to the formation of wiring, the volume of the barrier metal in the wiring increases relatively as a semiconductor device decreases in size. As a result, the part of the conductive film decreases. Thus, the resistance of the wiring increases as compared to the RIE wiring, or a so-called thin-wire effect is problematic.

[0016]

The above barrier metal has the problems that it hardly contributes to a reduction in wiring resistance and narrows

a distance between adjacent wiring and increases the capacitance between wiring.

[0017]

[Object of the Invention]

In the prior art, as described above, damascene wiring has the problems that the wiring resistance increases and the wiring-to-wiring capacitance increases although the conductive film is improved in yield and easily flattened and the semiconductor device can sufficiently be miniaturized.

[0018]

An object of the present invention is to provide a semiconductor device capable of preventing wiring resistance from increasing and preventing wiring-to-wiring capacitance from increasing and improving in performance, and a method for manufacturing the semiconductor device.

[0019]

[Means for Achieving the Object]

In order to achieve the above-described object, a semiconductor device according to the present invention is characterized by comprising: an insulation film provided above a semiconductor substrate; a conductive film selectively provided at least on a bottom of a groove section formed in the insulation film; and a wiring layer formed on the conductive film so as to have a space region between the wiring layer and a sidewall of the groove section.

[0020]

Further, the semiconductor device is characterized in that the conductive film has resistivity that is higher than

that of the wiring layer.

[0021]

The semiconductor device according to the present invention is characterized by comprising: an insulation film provided above a semiconductor substrate; a wiring layer buried in the insulation film; a first conductive film provided on a bottom of the wiring layer; and a second conductive film formed on a sidewall of the wiring layer, and different from the first conductive film.

[0022]

Further, the semiconductor device is characterized in that the second conductive film is made from a material different from that of the wiring layer.

[0023]

The semiconductor device according to the present invention is characterized by comprising: a first insulation film provided above a semiconductor substrate; a wiring layer buried in the first insulation film; a first conductive film provided on a bottom of the wiring layer; and a second insulation film formed on a sidewall of the wiring layer and different from the first insulation film.

[0024]

The semiconductor device according to the present invention is characterized by comprising: a first insulation film provided above a semiconductor substrate; a wiring layer buried in the first insulation film; a first conductive film provided on a bottom of the wiring layer; and a contact plug formed via the wiring layer and the second insulation film that

is different from the first insulation film.

[0025]

Further, a method of manufacturing a semiconductor device according to the present invention is characterized by comprising the steps of: forming an insulation film above a semiconductor substrate; forming a groove section in the insulation film; forming a conductive film along the interior surface of the groove section; forming a wiring layer by burying a first conductive material in the groove section via the conductive film; and selectively removing the conductive film formed on a sidewall portions of the groove section.

[0026]

In addition, the method of manufacturing a semiconductor device is characterized by comprising the step of selectively performing plasma processing on the conductive film formed on a bottom surface of the groove section before hand.

[0027]

The method of manufacturing a semiconductor device is characterized by further comprising the steps of: forming a second insulation film on the insulation film; and forming a space region between the wiring layer and the sidewall of the groove section from which the conductive film is removed.

[0028]

The method of manufacturing a semiconductor device is characterized by further comprising the step of burying a second insulation film in a region between the wiring layer and a sidewall of the groove section from which the conductive

film is removed.

[0029]

The method of manufacturing a semiconductor device is characterized by further comprising the step of burying a second conductive material in a region between the wiring layer and a sidewall of the groove section from which the conductive film is removed.

[0030]

The method of manufacturing a semiconductor device is characterized by further comprising the step of forming a spacer made from an insulation material in the interior wall surface of the groove section.

[0031]

The method of manufacturing a semiconductor device is characterized by further comprising the step of forming a contact in self-alignment with the insulation film with respect to the groove section.

[0032]

The method of manufacturing a semiconductor device according to the present invention is characterized by comprising the steps of: forming a first insulation film above a semiconductor substrate; forming a groove section in the first insulation film; forming a second insulation film on the interior surface of the groove section; forming a wiring layer by burying a conductive material in the groove section via the conductive film; and removing the second insulation film.

[0033]

Furthermore, the method of manufacturing a semiconductor

device is characterized by comprising the step of forming a third insulation film on the first insulation film and forming a space region in a region from which the second insulating film is removed.

[0034]

The method of manufacturing a semiconductor device is characterized by further comprising the step of burying the third insulation film in a region from which the second insulation film is removed.

[0035]

According to the semiconductor device and the method of manufacturing the same described above, the sidewall portions of a groove section can effectively be used. Thus, the wiring resistance can easily be decreased and so can be the wiring-to-wiring capacitance.

[0036]

[Embodiments of the Invention]

Embodiments of the present invention will now be described with reference to the accompanying drawings.

[0037]

(First Embodiment)

FIG. 1 schematically shows a cross section of a semiconductor device having a damascene wiring according to a first embodiment of the present invention.

[0038]

A silicon oxide film (insulation film/first insulation film) 12 is provided on a semiconductor substrate 11, and a wiring pattern groove (groove section) 13 is formed in

a surface portion of the silicon oxide film 12. A barrier metal film (conductive film/first conductive film) 14 is selectively formed on the bottom of the groove 13. A wiring layer 16, which is constituted of a conductive film (first conductive material), is provided on the barrier metal film 14 in such a manner as being almost flush with the upper surface of the groove 13. A hollow section (space region) 15 is formed between each sidewall of the groove 13 and each side of the wiring layer 16. A plasma SiO_2 film (second/third insulation film) 17 is formed on the entire surface of the silicon oxide film 12.

[0039]

The hollow section 15 is obtained by selectively removing a barrier metal film formed on each sidewall of the groove 13 and further forming the plasma SiO_2 film 17.

[0040]

The above structure results in a damascene wiring with a hollow section 15 of low dielectric constant on its wall surfaces. Even when a damascene technique is used for forming a wiring, the wiring-to-wiring capacitance can be reduced effectively maintaining a high yield.

[0041]

A method of forming a damascene wiring with the above structure will now be described with reference to FIG. 2.

[0042]

First, for example, a wiring pattern groove 13 is formed in a silicon oxide film 12 provided on a semiconductor substrate 11 by known lithography and RIE (see FIG. 2(a)).

[0043]

Then, a TiN film 14' serving as a barrier metal film 14 is deposited on the entire surface by CVD (Chemical Vapor Deposition) using an organic raw-material gas (see FIG. 2(b)).

[0044]

Of the TiN film 14', only the quality of the TiN film 14a' exposed to the bottom of the groove 13 is changed by anisotropic plasma processing (see FIG. 2(c)).

[0045]

The just-deposited TiN film 14' contains a large number of organic impurities such as carbon. The TiN film is low in density and very unstable. Therefore, the TiN film 14' should be changed to TiN film 14a' having a dense quality by scattering the impurities by plasma processing.

[0046]

Since the plasma processing is anisotropic when performing the plasma processing, the TiN film 14b' formed on the sidewalls of the groove 13 is hardly exposed to plasma. The TiN film 14b' formed on the sidewalls of the groove 13 remains unstable to cause a difference in quality between the TiN film 14b' and the TiN film 14a' formed on the bottom of the groove 13.

[0047]

Subsequently, a conductive film (e.g., W) 16′ which is to serve as a wiring layer 16, is deposited on the entire surface by CVD to completely fill the groove 13 (see FIG. 2(d)).

[0048]

A wiring layer 16 is then formed by removing the

conductive film 16' and TiN film 14' until the top surface of the silicon oxide film 12 is exposed to obtain a flat surface by CMP (see FIG. 2(e)).

[0049]

Next, the TiN film 14b' is selectively removed from the sidewalls of the groove 13 by SC-2 (Hydrochloric acid / Hydrogen peroxide aqueous solution) processing. The barrier metal film 14 is thus formed only from the TiN film 14a' on the bottom of the groove 13 (see FIG. 2(f)). Since the TiN film 14b' on the sidewalls of the groove 13 remains unstable, the rate of wet etching is high and the TiN film 14a' can selectively be removed from the bottom of the wiring layer 16 and the groove 13.

[0050]

After that, a plasma SiO_2 film 17 is deposited on the entire surface by plasma CVD. A hollow section 15 is formed between each side of the wiring layer 16 and each sidewall of the groove 13. Thus, a semiconductor device having a damascene wiring as shown in FIG. 1 can be obtained.

[0051]

In the first embodiment, poor burying characteristics of the plasma SiO_2 film 17 prevent the film 17 from being buried into an etching region (space region) 15a excluding the TiN film 14b'. Consequently, the hollow section 15, which is capable of effectively reducing the wiring-to-wiring capacitance, can be formed.

[0052]

In the above first embodiment, the etching region

15a from which the barrier metal film 14 is partly removed using the film the coverage characteristics of which are poor, is used effectively as the hollow section 15. The present invention is not limited to this feature. For example, the etching region 15a can be filled with an insulation film (second/third insulation film) 21, as illustrated in FIGS. 3(a) to 3(c).

[0053]

(Second Embodiment)

More specifically, after the step shown in FIG. 2(f) of the first embodiment, an insulation film 21 whose burying characteristics are improved (For example, a TEOS (Tetra Ethyl or the Silicate) film formed by plasma CVD or an SOG (Spin On Glass) film formed by coating) is deposited on the entire surface in place of the plasma SiO_2 film 17. By flattening the insulation film 21 by CMP, the etching region 15a is buried with the insulation film 21.

[0054]

In the second embodiment, when a damascene wiring is formed, regions (sidewalls of groove 13) in which the barrier metal film 14 is originally provided can be used as insulation regions by substituting the insulation film 21. If, therefore, the wiring pattern groove 13 is widened in advance by the thickness of the barrier metal film 14, an increase in wiring resistance due to microfabrication can be suppressed effectively.

[0055]

(Third Embodiment)

FIGS. 4(a) to 4(c) schematically show a process of manufacturing a semiconductor device having a damascene wiring according to a third embodiment of the present invention. The process up to the step of selectively removing the TiN film 14b' from the sidewalls of the groove 13 is the same as that shown in FIGS. 2(a) to 2(f). The steps subsequent thereto will now be described below.

[0056]

The TiN film 14b' is selectively removed from the sidewalls of the groove 13 by SC-2 processing to form a barrier metal film 14 (see FIG. 4(a)). Then, a W film (second conductive film/second conductive material) 31 is deposited on the entire surface by sputtering (see FIG. 4(b)). The W film may be deposited by CVD.

[0057]

Next, using CMP, the W film 31 is removed until the top surface of a silicon oxide film 12 is exposed so that the resultant structure is flattened. Thus, an etching region 15a between each side of the wiring layer 16 and each sidewall of the groove 13 is completely filled with the W film 31 (see FIG. 4(c)).

[0058]

In the third embodiment, too, regions (sidewalls of the groove 13) in which the barrier metal film 14 is originally provided can be used as wiring regions by substituting the W film 31 for. The line width of a damascene wiring can thus be

increased by the thickness of the barrier metal film 14. In other words, the region corresponding to the thickness of the barrier metal film 14 can be used as a wiring without waste. As a result, a semiconductor device with the above damascene wiring can be microfacbricated without increasing the resistance of wiring.

[0059]

Not only the W film but also any other conductive film can be used as the second conductive film/second conductive material that is buried into the etching region 15a.

[0060]

In the first to third embodiments, a spacer (second /third insulation film) can be provided, e.g., on each sidewall of the groove 13 in addition to the barrier metal film.

[0061]

(Fourth Embodiment)

FIGS. 5(a) to 5(g) schematically show a process of manufacturing a semiconductor device having a damascene wiring according to a fourth embodiment of the present invention. The fourth embodiment will now be described in brief, taking the first embodiment in which the hollow section 15 is provided between each side of the wiring layer 16 and each sidewall of the groove 13 as an example.

[0062]

A wiring pattern groove 13 is formed in a silicon oxide film 12 formed on a semiconductor substrate 11 by known lithography and RIE. After that, a SiN (silicon nitride) film serving as a second/third insulation film is deposited on the

surface of the silicon oxide film 12 by CVD. Then, the SiN film is selectively removed by anisotropic etching and left only on each sidewall of the groove 13, thereby forming a spacer 41 (see FIG. 5(a)).

[0063]

If the same steps as those of FIGS. 2(b) et seq. are executed after the above step, a semiconductor device having a damascene wiring can be obtained in which the spacer 41 is provided on each sidewall of the groove 13 and the hollow section 15 is formed between the spacer 41 and each side of the wiring layer 16.

[0064]

The structure of the fourth embodiment can produce an advantage as well as that of the first embodiment. Not only wiring-to-wiring capacitance can effectively be reduced maintaining a high yield, but also wiring-to-wiring insulating characteristics can be improved further. The semiconductor device can thus be microfabricated more greatly.

[0065]

(Fifth Embodiment)

FIGS. 6(a) to 6(e) schematically show a process of manufacturing a semiconductor device having a damascene wiring according to a fifth embodiment of the present invention. The fifth embodiment is directed to a case where the above-described hollow section 15 is formed by removing the spacer 41, which is formed on each sidewall of the groove 13 in the fourth embodiment.

[0066]

A silicon oxide film 12 is formed on a semiconductor substrate 11 and a wiring pattern groove 13 is formed in the silicon oxide film 12 by known lithography and RIE (see FIG. 6(a)).

[0067]

After that, a SiN film serving as a third insulation film is deposited on the surface of the silicon oxide film 12 by CVD. The SiN film is selectively removed by anisotropic etching and left only on each sidewall of the groove 13, resulting in spacers 41 (see FIG. 6(b)).

[0068]

A TiN film serving as a barrier metal film 14 is deposited on the entire surface by CVD which uses an organic raw-material gas and a W film serving as a wiring layer 16 is deposited by CVD thereon. The resultant structure is flattened by CMP until the top surface of the silicon oxide film 12 is exposed, resulting in the barrier metal film 14 and the wring layer 16 (see FIG. 6(c)). Additionally, the TiN film may be deposited by spattering.

[0069]

Wet etching in phosphoric acid allows the spacers 41 to be selectively removed from the sidewalls of the groove 13 (see FIG. 6(d)).

[0070]

A plasma SiO_2 film 17 is deposited on the entire surface, e.g., by plasma CVD (see FIG. 6(e)). The film 17 inhibits the etching region 15a selectively excluding the spacers 41 from

being filled completely. Consequently, a semiconductor device having a damascene wiring can be manufactured in which a hollow section 15 is provided along each sidewall of the groove 13.

[0071]

The etching region 15a is therefore prevented from being filled completely using a film of poor coverage characteristics such as plasma SiO_2 on purpose. As in the first embodiment, the hollow section 15 can easily be formed along each sidewall of the groove 13 excluding the spacers 41. The section 15 allows the wiring-to-wiring capacitance to be reduced effectively.

[0072]

According to the fifth embodiment, the hollow section 15 can be formed along each side of the wiring layer 16 with good controllability even when the barrier metal film 14 is difficult to selectively remove from the wiring layer 16 or even though no anisotropic plasma processing is executed.

[0073]

(Sixth Embodiment)

FIGS. 7(a) to 7(f) schematically show a process of manufacturing a semiconductor device having a damascene wiring according to a sixth embodiment of the present invention. The sixth embodiment is directed to a DRAM cell using a stacked capacitor. The process up to the step of forming the wiring layer 16 is the same as that shown in FIGS. 2(a) to 2(e) of the first embodiment. The steps subsequent thereto will now be described below.

[0074]

After the wiring layer 16 is formed using CMP by flattening the conductive film 16' and the TiN film 14' deposited on the entire surface until the upper surface of the silicon oxide film 12 is exposed (see FIG. 7(a)), the wiring layer 16 is selectively etched by RIE using Cl_2 gas. Thus, a bit line 51 is formed (see FIG. 7(b)).

[0075]

As in the first embodiment, a TiN film 14b' is selectively removed from each sidewall of the groove 13 by SC-2 processing. Thus, a barrier metal film 14 is formed from only the TiN film 14a' on the bottom of the groove 13 (see FIG. 7(c)).

[0076]

A silicon nitride film 52 is deposited on the entire surface by CVD. An etching region 15a excluding the TiN film 14b' and a step region (space region) 15b formed by etching the wiring layer 16 are completely filled with the silicon nitride film 52. Then, a surface of the film 52 is flattened by CMP, simultaneously forming a sidewall 53 in the etching region 15a (see FIG. 7(d)).

[0077]

A photoresist film (not shown) is formed on the silicon oxide film 12 and patterned by known lithography. The silicon oxide film 12 is etched to form a contact hole 54 reaching the semiconductor substrate 11. The photoresist film and silicon nitride film 52 are removed by RIE using C_4F_8 gas having a high selection ratio. The contact hole 54 is formed in

self-alignment with the silicon nitride film 52 (see FIG. 7(e)).

[0078]

After the photoresist film is eliminated, a TiN film serving as a barrier metal film 55 and a conductive film (e.g., tungsten) serving as a storage node contact 56 are deposited on the entire surface by CVD to fill the contact hole 54 completely. By flattening the structure by CMP until the top surface of the silicon oxide film 12 is exposed, a contact plug is formed of the barrier metal film 55 and the storage node contact 56 (see FIG. 7(f)).

[0079]

After that, a capacitor and a plate electrode are formed in the same manner as those of the normal DRAM cell.

[0080]

According to the sixth embodiment, the storage node contact 56 can be formed in self-alignment with the bit line 51 in a DRAM cell using a stacked capacitor. No margin for alignment is required for forming the contact hole 54. Therefore, a distance between bit lines 51 can sufficiently be reduced and the chip size can easily be decreased.

[0081]

In particular, since sidewalls 53 for insulating the bit lines 51 and the storage contact 56 from each other are formed at the same time when the silicon nitride film 52 is buried. The number of manufacturing steps can thus be reduced. Moreover, the regions (15a) that correspond to those occupied by the barrier metal can effectively be used. Consequently,

a so-called thinning effect of increasing the resistance of the bit lines 51 can easily be suppressed.

[0082]

In the embodiment described above, the step region 15b (bit line 51) is formed by selectively etching the wiring layer 16 and then the TiN film 14b' is selectively removed from each sidewall of the groove 13. The present invention is not limited to this structure. For example, the bit line 51 can easily be formed after the TiN film 14b' is selectively removed.

[0083]

If the present invention is applied to the DRAM cell using a stacked capacitor, a spacer (second/third insulation film) 41 can be provided at least between the groove 13 and the contact hole 54, as illustrated in FIG. 8. In this case, a hollow section 15 can be formed between the bit line 51 and the spacer 41 as in the fourth embodiment (see FIG. 5). The wiring-to-wiring capacitance between the bit line 51 and the storage node contact 56 can effectively be reduced.

[0084]

As described above, the sidewalls of the wiring pattern groove can effectively be utilized.

[0085]

In other words, a hollow section is formed, an insulation film is buried, or a conductive film is buried between each sidewall of the wiring pattern groove and each side of the wiring layer in the damascene wiring. When the hollow section is formed, the wiring-to-wiring capacitance can be prevented

from increasing. When the insulation film is buried, the wiring-to-wiring insulation characteristics can be improved. When the conductive film is buried, an increase in wiring resistance due to the thinning effect can be prevented. This is very effective in miniaturizing a semiconductor device and decreasing the size of a chip. The suppression of the thinning effect effectively allows the wiring resistance to decrease and allows the wiring-to-wiring capacitance to be reduced, with the result that the semiconductor device can easily be improved in performance.

[0086]

In the foregoing embodiments of the present invention, a hollow section or the like is provided along each sidewall of the wiring pattern groove. Alternatively, the hollow section can be provided only on the sidewall adjacent to at least another damascene wiring.

[0087]

Needless to say, the present invention can be practiced in various modifications without departing from the spirit and scope thereof.

[0088]

[Advantage of the Invention]

According to the present invention described in detail above, there can be provided a semiconductor device capable of preventing a wiring resistance and a wiring-to-wiring capacitance from increasing and improving in performance and a method of manufacturing the semiconductor device.

[Brief Description of the Drawings]

[FIG. 1]

A schematic cross-sectional view showing a main portion of a semiconductor device having a damascene wiring according to a first embodiment of the present invention.

[FIG. 2]

Cross-sectional views showing a process of forming the damascene wiring according to the first embodiment of the present invention.

[FIG. 3]

Cross-sectional views showing a process of manufacturing a damascene wiring according to a second embodiment of the present invention.

[FIG. 4]

Cross-sectional views showing a process of manufacturing a damascene wiring according to a third embodiment of the present invention.

[FIG. 5]

Cross-sectional views showing a process of manufacturing a damascene wiring according to a fourth embodiment of the present invention.

[FIG. 6]

Cross-sectional views showing a process of manufacturing a damascene wiring according to a fifth embodiment of the present invention.

[FIG. 7]

Cross-sectional views showing a process of manufacturing an example of a damascene wiring according to a sixth

embodiment of the present invention, which is applied to a DRAM cell using a stacked capacitor.

[FIG. 8]

A cross-sectional view showing another configuration example of the damascene wiring according to the sixth embodiment of the present invention, which is applied to the DRAM cell using a stacked capacitor.

[FIG. 9]

Cross-sectional views showing a process of manufacturing a damascene wiring in order to describe a prior art technique and its problems.

[FIG. 10]

Cross-sectional views showing a damascene wiring and an RIE wiring having the same line width in the prior art technique for purposes of comparison.

[Explanation of Reference Symbols]

11	… Semiconductor substrate,
12	… Silicon oxide film,
13	… Wiring pattern groove,
14	… Barrier metal film,
14′, 14a′, 14b′	… TiN film,
15	… Hollow section,
15a	… Etching region,
15b	… Step region,
16	… Wiring layer,
16′	… Conductive film (W),
17	… Plasma SiO_2 film,
21	… Insulation film,

31 … W film,

41 … Spacer,

51 … Bit line,

52 … Silicon nitride film,

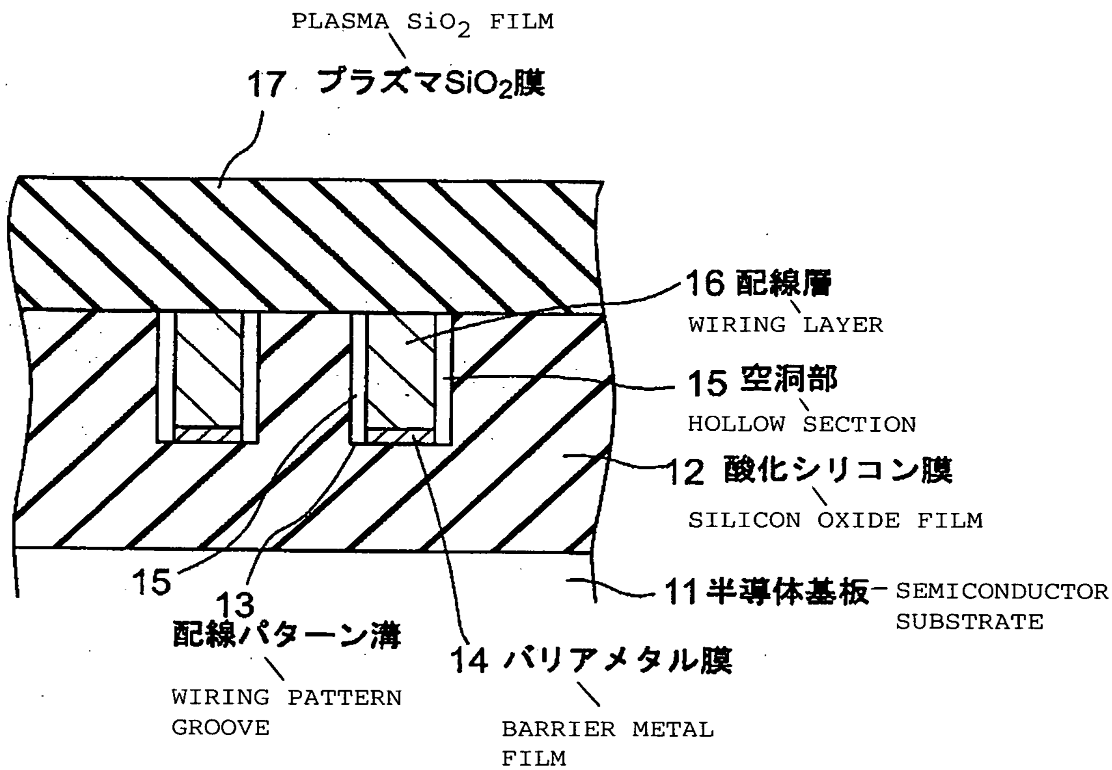
53 … Sidewall,

54 … Contact hole,

55 … Barrier metal film,

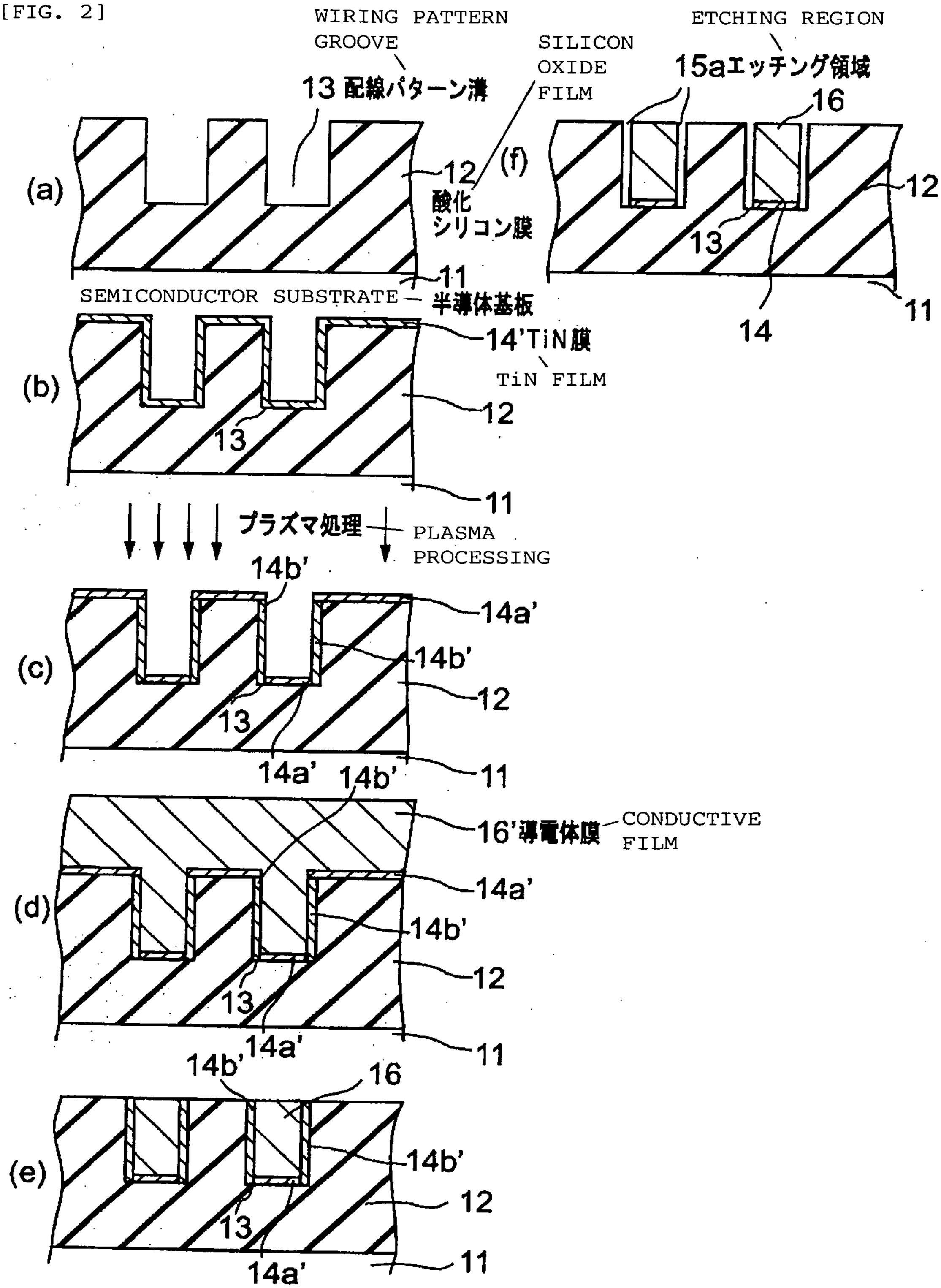
56 … Storage node contact.

【書類名】 図面
[NAME OF DOCUMENT] DRAWINGS
【図１】
[FIG. 1]



【図２】

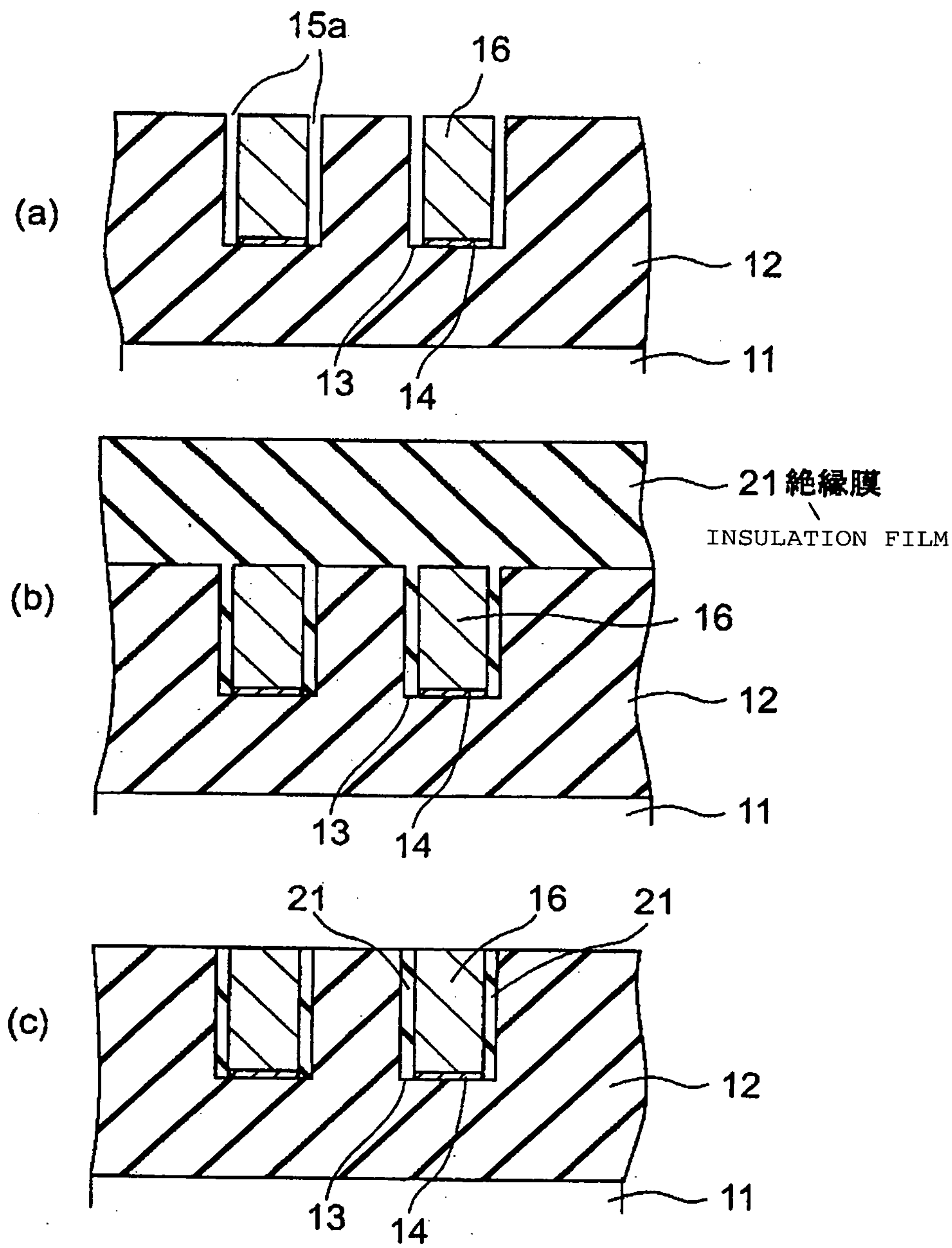
[FIG. 2]



WIRING PATTERN GROOVE
13 配線パターン溝
SILICON OXIDE FILM
ETCHING REGION
15aエッチング領域
16
(a)
12
(f)
酸化シリコン膜
12
13
11
SEMICONDUCTOR SUBSTRATE
半導体基板
11
14
14'TiN膜
TiN FILM
(b)
12
13
11
プラズマ処理
PLASMA PROCESSING
14b'
14a'
(c)
14b'
12
13
14a'
11
14b'
16'導電体膜
CONDUCTIVE FILM
14a'
(d)
14b'
12
13
14a'
11
14b'
16
(e)
14b'
12
13
11
14a'

【図3】

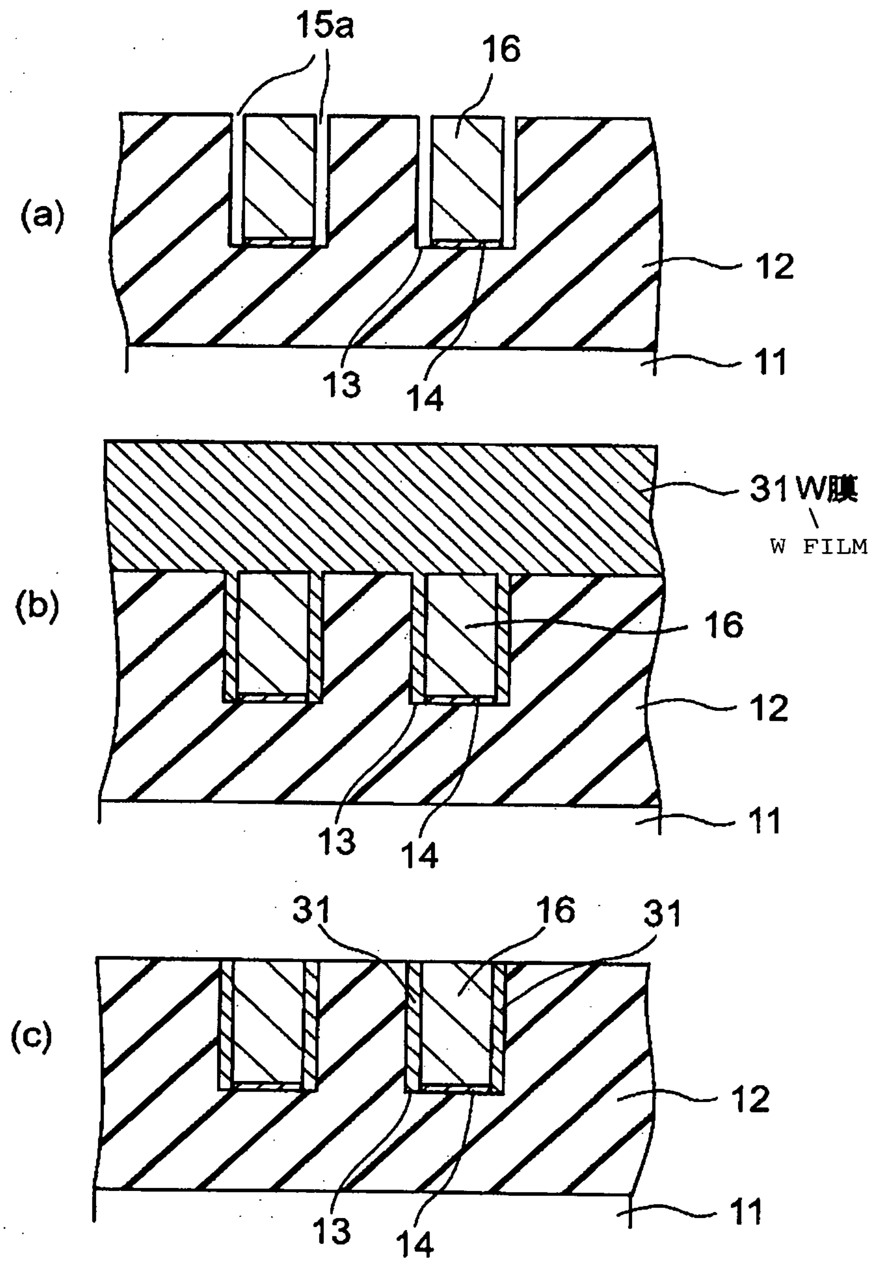
[FIG. 3]



15a
16
(a)
12
11
13
14
21絶縁膜
INSULATION FILM
(b)
16
12
11
13
14
21
16
21
(c)
12
11
13
14

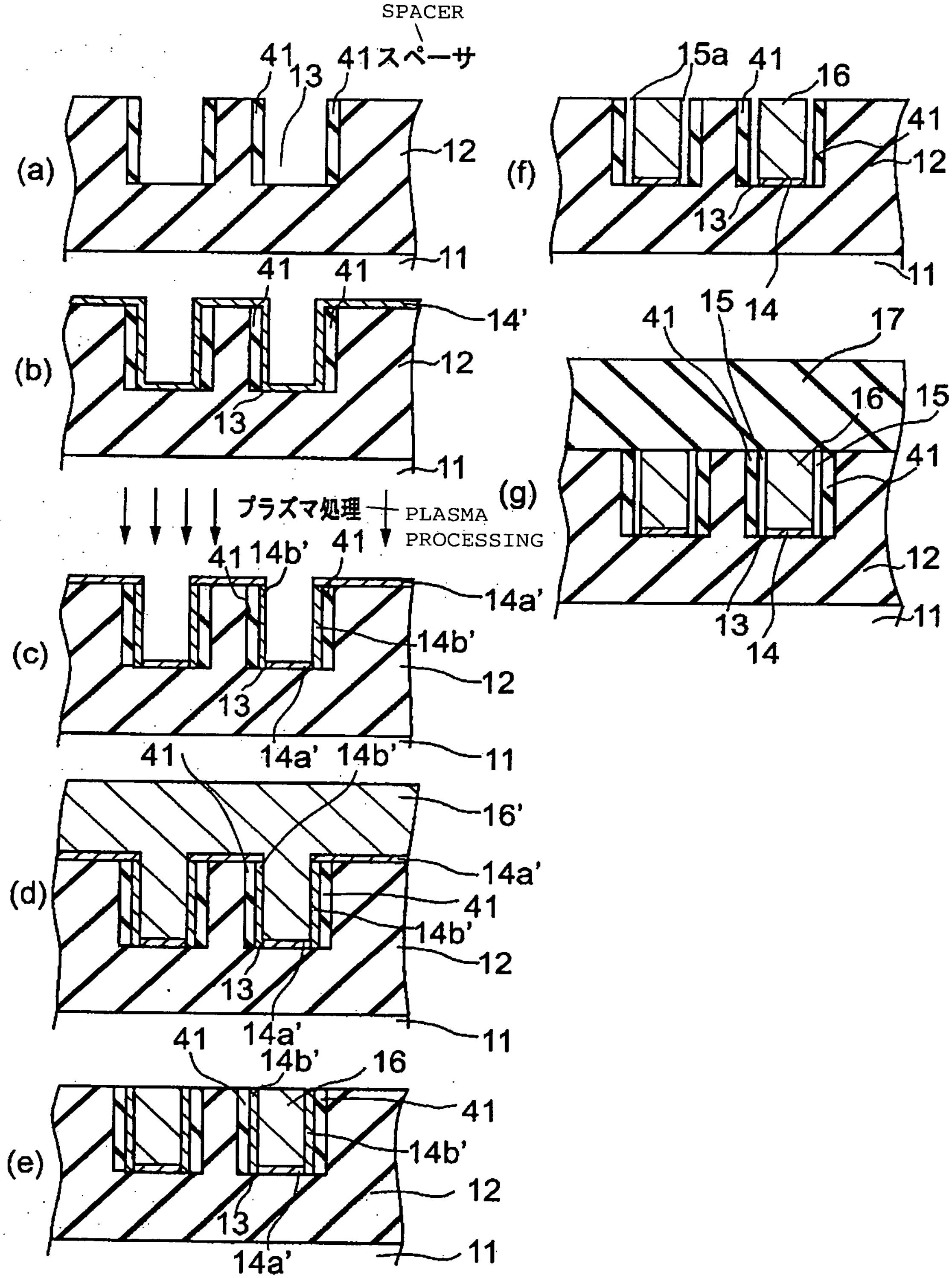
【図４】

[FIG. 4]



【図５】

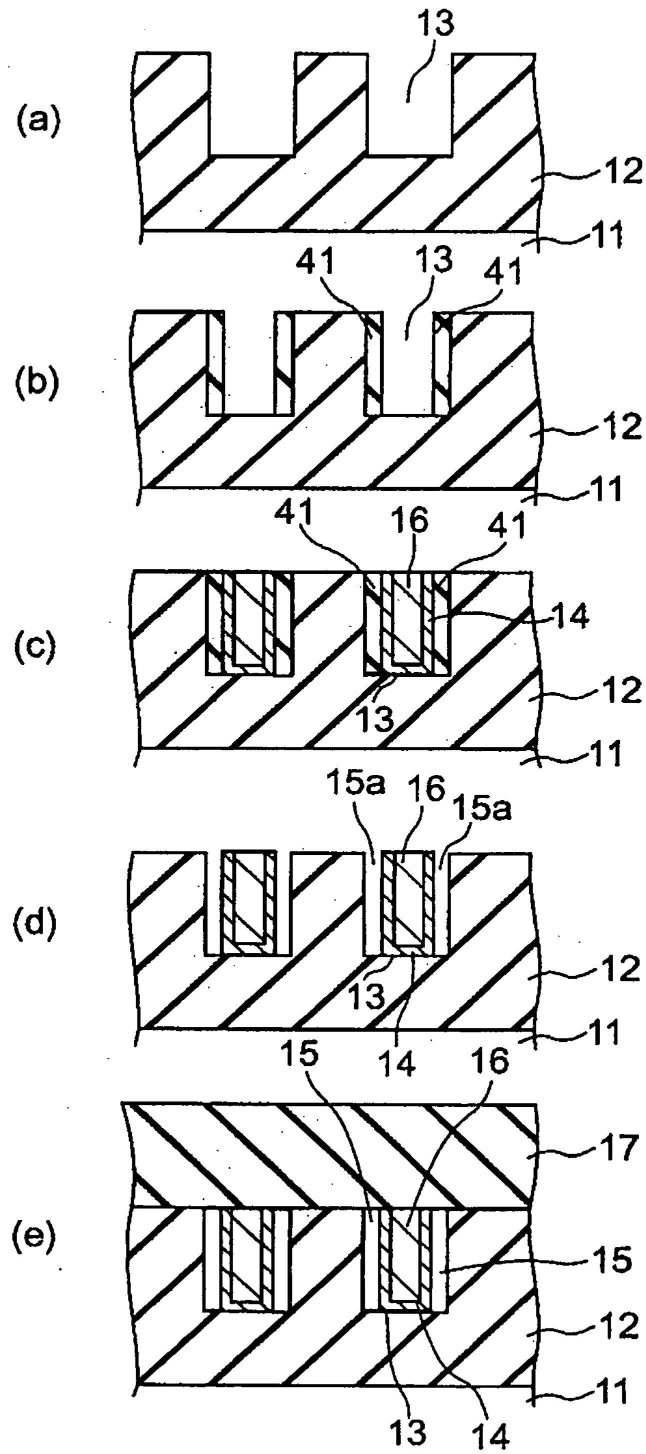
[FIG. 5]



SPACER
41
13
41スペーサ
12
11
(a)
41
41
14'
12
13
11
(b)
プラズマ処理
PLASMA
PROCESSING
41
14b'
41
14a'
14b'
12
13
14a'
11
(c)
41
14b'
16'
14a'
41
14b'
12
13
14a'
11
(d)
41
14b'
16
41
14b'
12
13
14a'
11
(e)
15a
41
16
41
12
13
14
11
(f)
41
15
14
17
16
15
41
12
13
14
11
(g)

【図６】

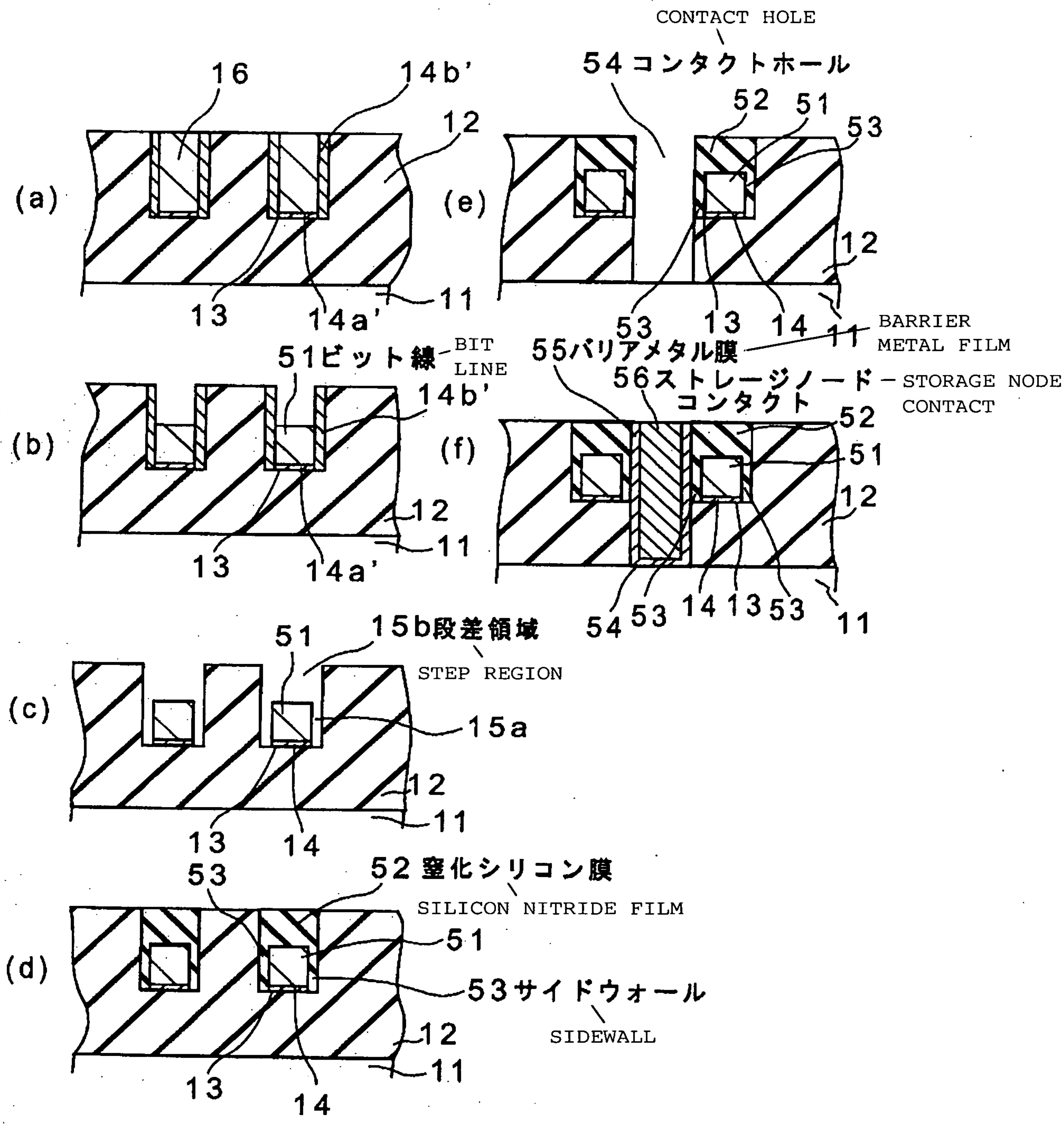
[FIG. 6]



(a)
13
12
11
(b)
41
13
41
12
11
(c)
41
16
41
14
12
13
11
(d)
15a
16
15a
12
13
11
14
(e)
15
16
17
15
12
11
13
14

【図７】

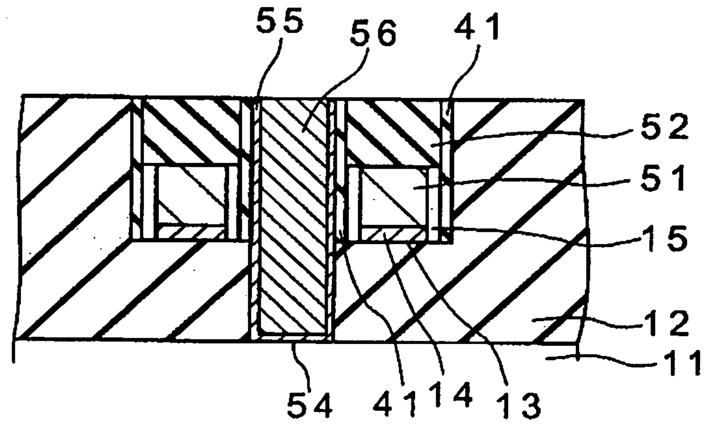
[FIG. 7]



(a)
16
14b'
12
13
14a'
11
(b)
51ビット線
BIT LINE
14b'
12
13
14a'
11
(c)
51
15b段差領域
STEP REGION
15a
12
13
14
11
(d)
53
52 窒化シリコン膜
SILICON NITRIDE FILM
51
53サイドウォール
SIDEWALL
12
13
14
11
(e)
CONTACT HOLE
54コンタクトホール
52
51
53
12
53
13
14
11
(f)
BARRIER METAL FILM
55バリアメタル膜
56ストレージノードコンタクト
STORAGE NODE CONTACT
52
51
12
54
53
14
13
53
11

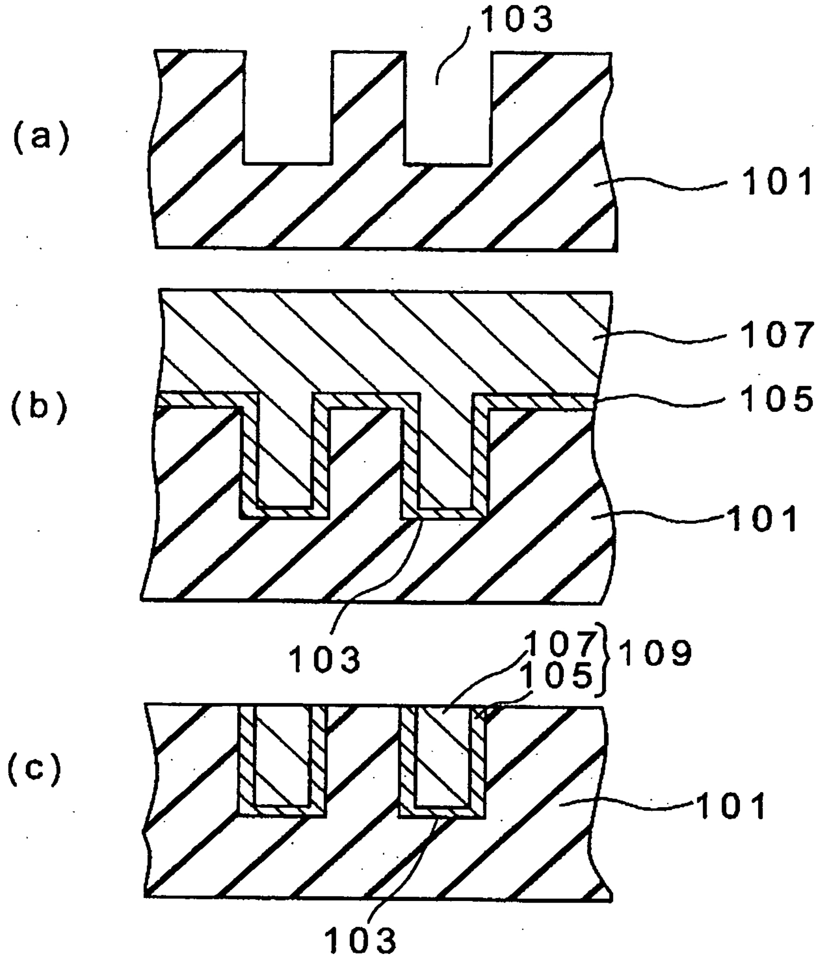
【図８】

[FIG. 8]



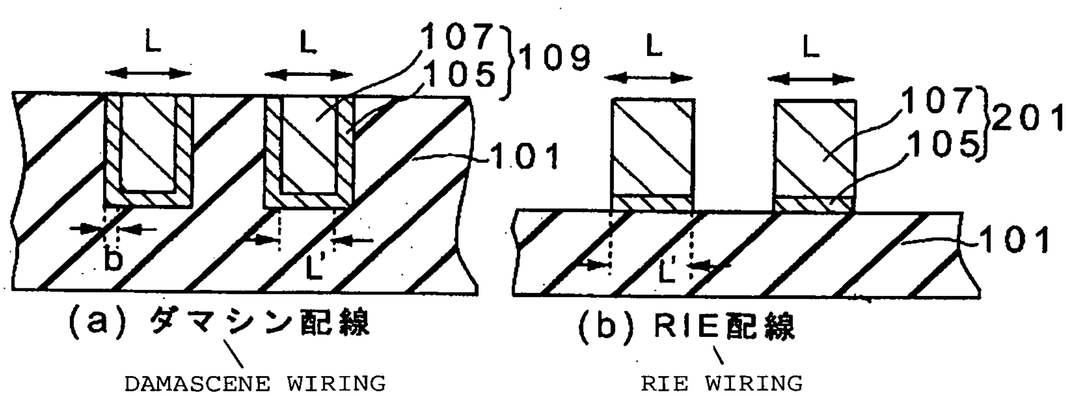
【図９】

[FIG. 9]



【図１０】

[FIG. 10]



[Document] ABSTRACT

[Abstract]

[Object] The present invention is mainly characterized in that, in a semiconductor device having a wiring of damascene structure, the wiring-to-wiring capacitance can effectively be reduced.

[Means for Achieving the Object] For example, a wiring pattern groove 13 is formed in a surface of a silicon oxide film 12 provided above a semiconductor substrate 11. A barrier metal film 14 is selectively formed on the bottom of the groove 13. A wiring layer 16 is formed with a hollow section 15 interposed between the layer 16 and each sidewall of the groove 13 on the barrier metal film 14. With this arrangement, a damascene wiring having a hollow section 15 whose dielectric constant is low is formed on each sidewall of the groove.

[Elected Figure] FIG. 1